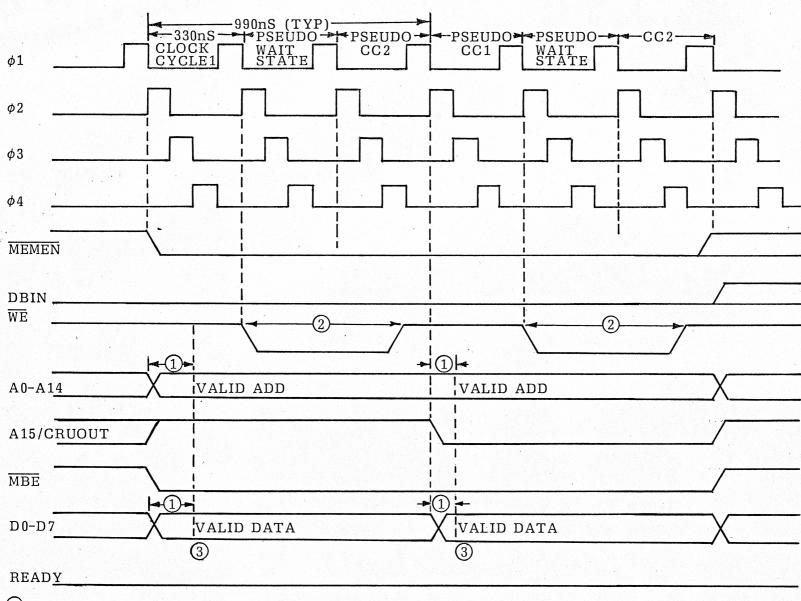


①-SETTLING TIME= 100nS (MIN)

(3)-SETUP TIME FOR 9900= 60nS (MIN)

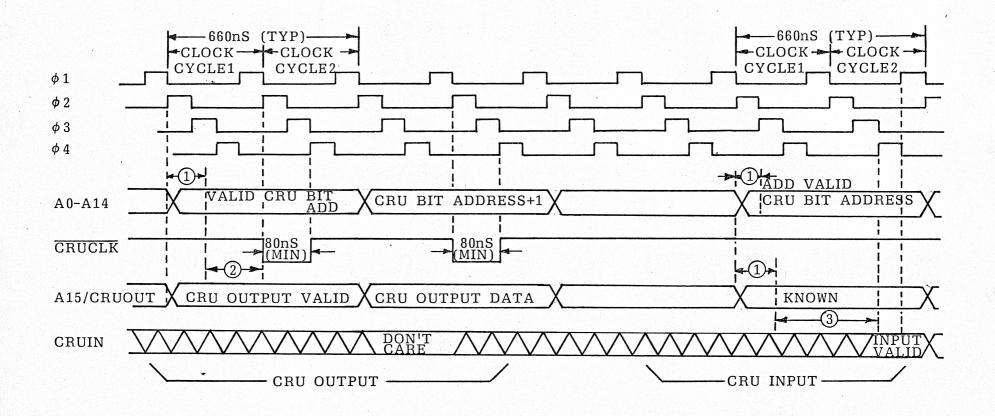
<sup>2-</sup>ACCESS TIME FOR DSR ROM + DATA Ts + DATA BUFF DELAY (PEREFERAL + MAINFRAME) =650nS (MAX)



1)-SETTLING TIME= 100nS (MIN) 2)-WE PULSE WIDTH= 660nS (TYP)

(3)-VALID DATA

FIRURE C I/O WRITE TIMING



1 -SETTLING TIME 100nS (MIN)

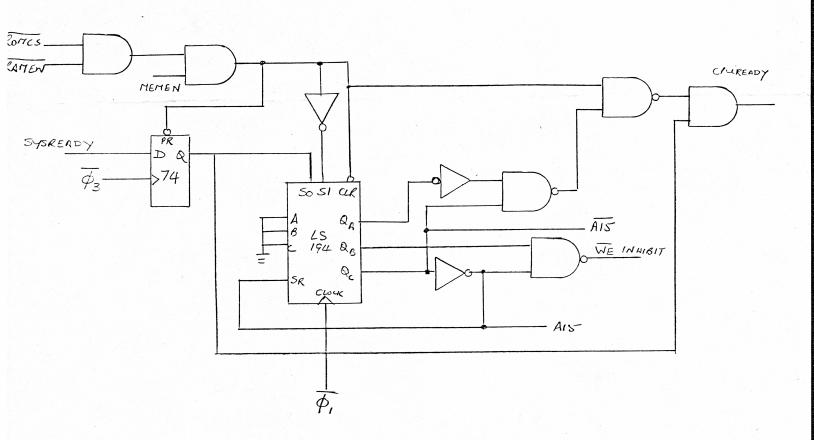
(2)-ADD VALID TO CRUCLK =220nS (TYP) (3)-ADD VALID TO VALID CRUIN =400nS (MAX)

FIGURE D CRU TIMING

1/31/70

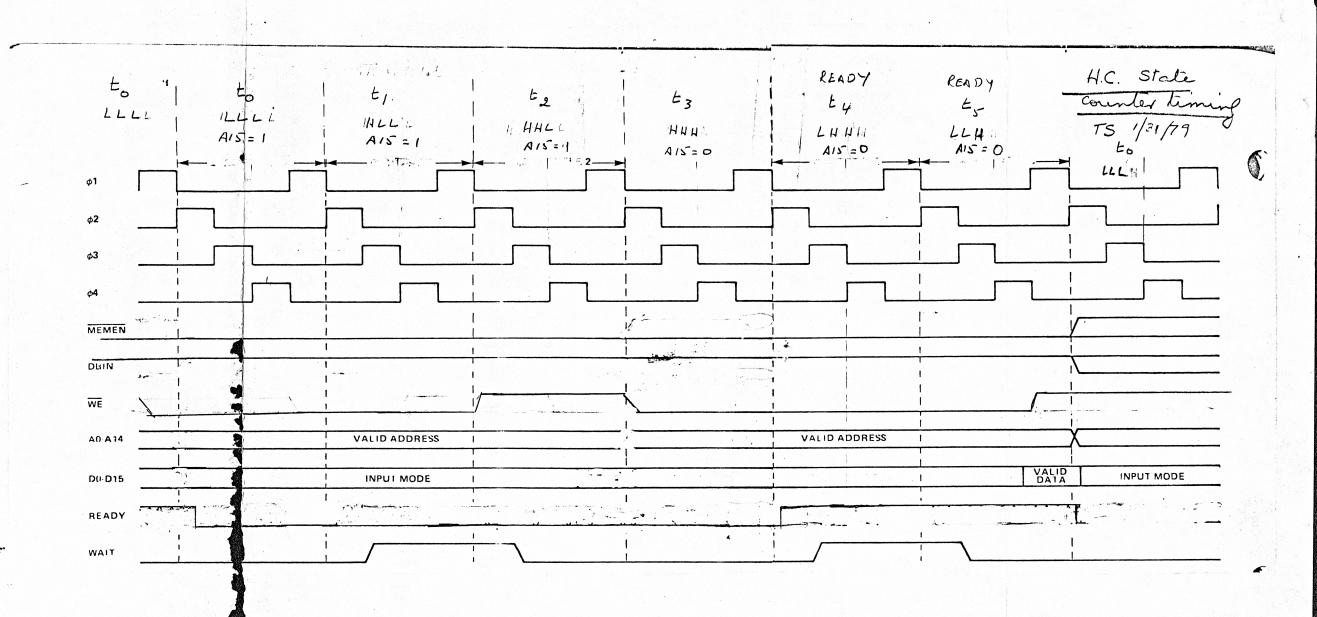
Herb Taylor
Tack Anderson
Allan Lawson
C.B. Wilson

rom: Tamin Shipchandler



Now that the trial and tribulations of implementing and cherking out the above state logic is complete, let us plan I on installing it in all simulators and systems. The state logic is currently working in simulator 4. A timing diagram is allowed that your un.

Thanks.



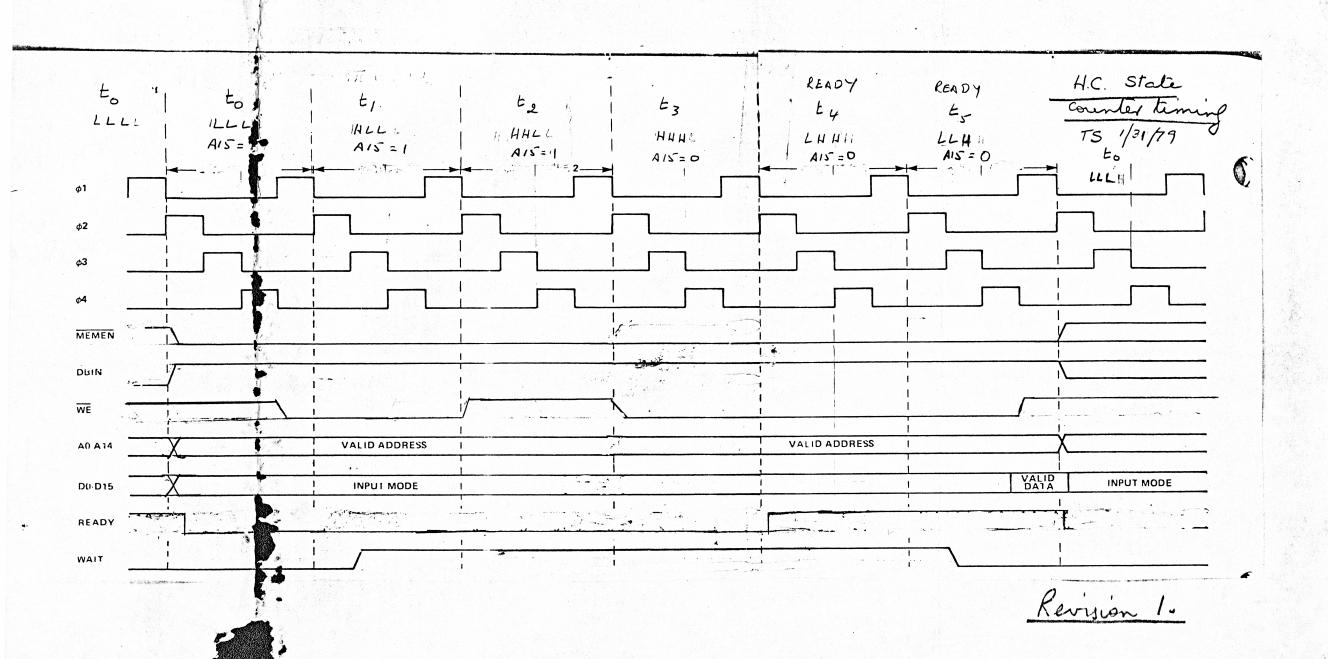
To france 0H Herb Taylor Jack Anderson Alan Lawson C.B wloon -

From: Tamen Shepchandle

Sulgest: my memo and timing diagram of 1/31/53 Due to an oversight on my part, minor errors crept into He timing diagram in the MEMEN, WE , DBIN and WAIT Synals. Please correct as attached.

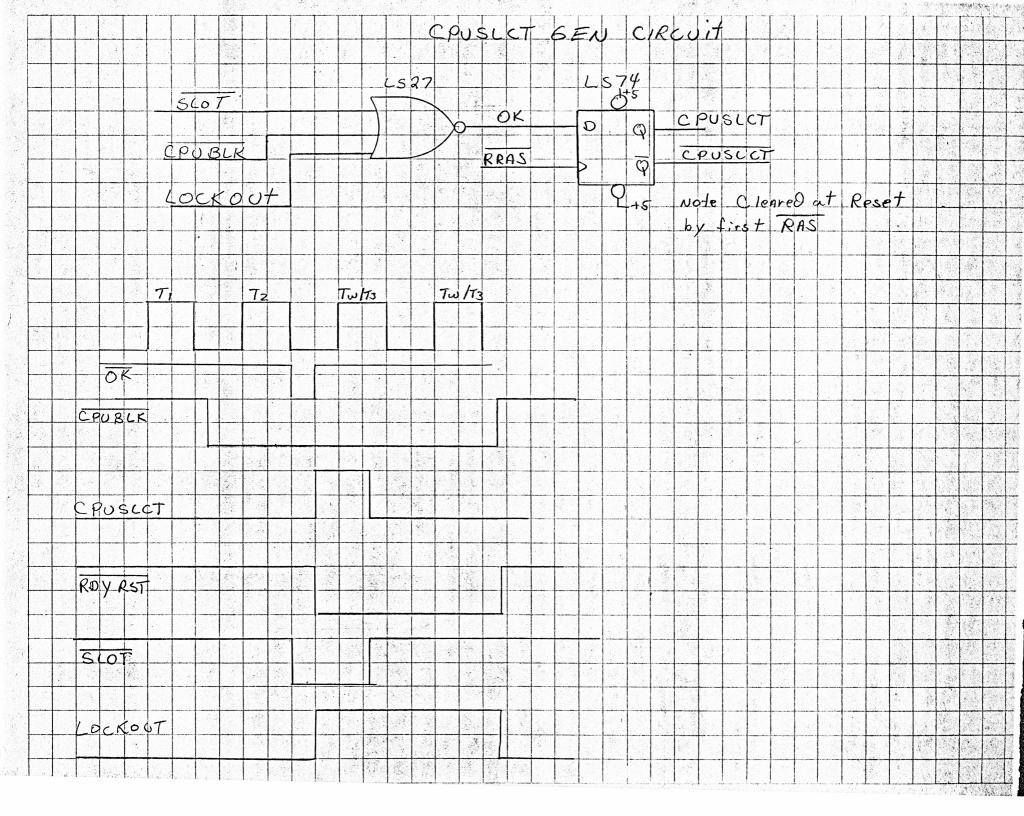
Thanks

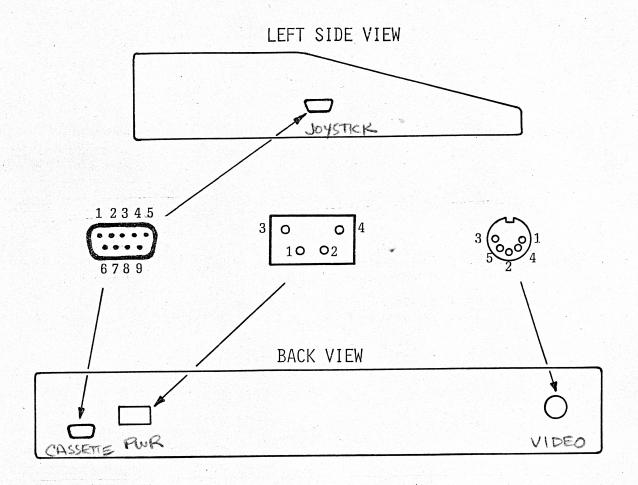
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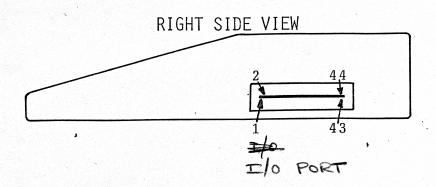


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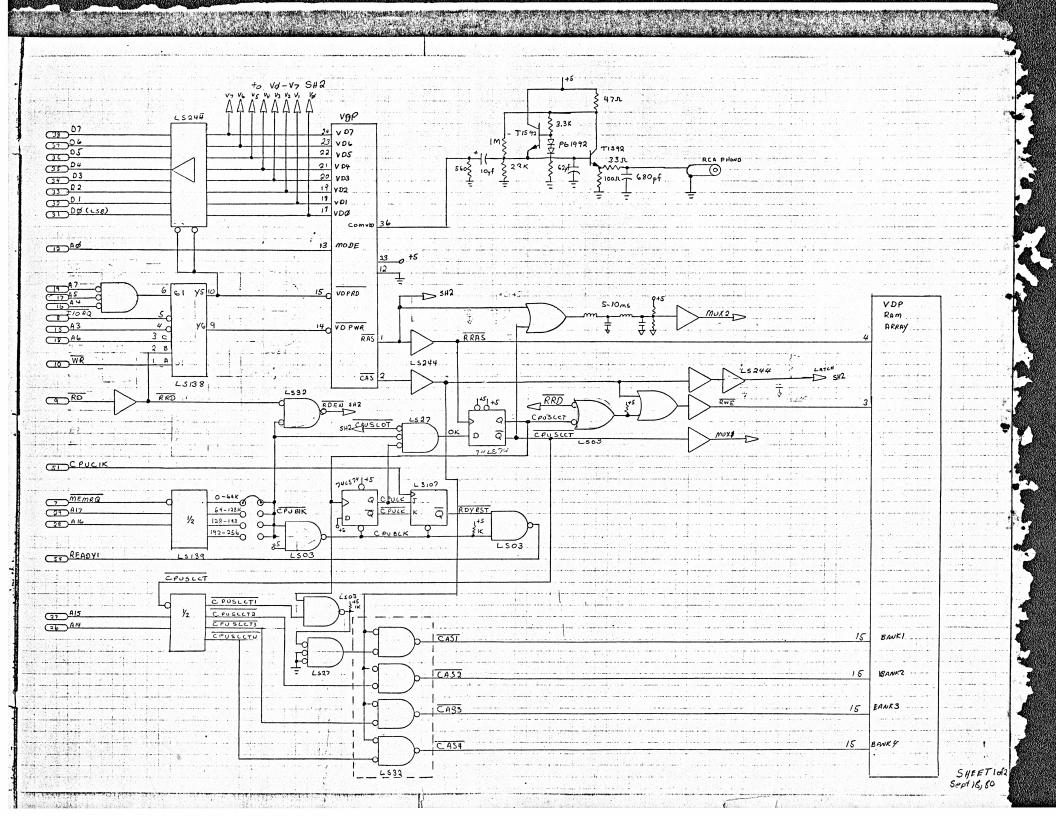


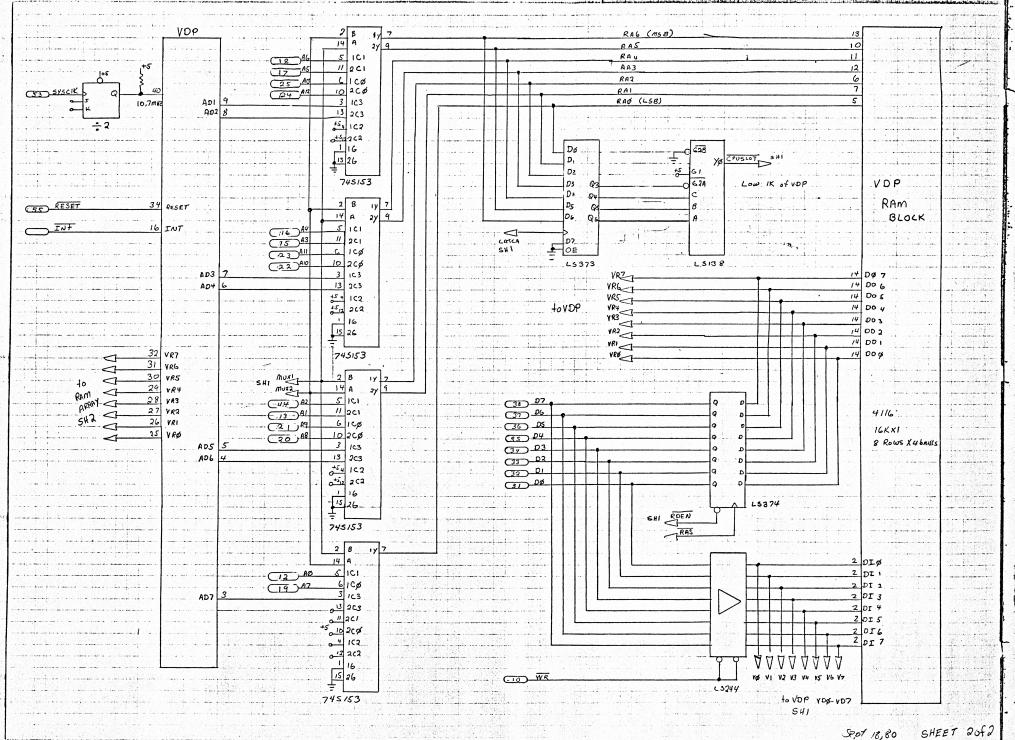




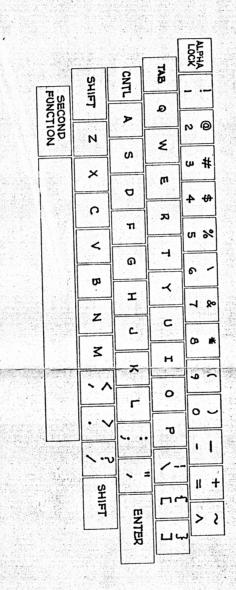
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